Amendments to the Specification

Please amend the following paragraphs / sections as indicated.

Please amend the paragraph beginning on page 1, line 6, as follows:

This application is a continuation of U.S. Patent Application No. 10/183,552, filed June 28, 2002, which is a continuation of U.S. Patent Application No. 09/547,968, filed April 12, 2000, which is a continuation-in-part of U.S. Patent Application No. 09/493,942, filed January 28, ~~2000;~~ 2000, which is a continuation-in-part of U.S. Patent Application No. 09/483,551, filed January 14, ~~2000;~~ 2000, which is a continuation-in-part of U.S. Patent Application No. ~~09/439,101~~ 09/439,101, filed November 12, ~~1999;~~ 1999, the disclosures of which [[is]] are incorporated herein by reference in all of their entireties.

Please amend the paragraph beginning on page 1, line 12, as follows:

~~This application~~ U.S. Patent Application No. 09/547,968 claims the benefit of U.S. Provisional Application No. 60/129,133, filed April 13, ~~1999;~~ 1999, the contents of which is hereby incorporated by reference in its entirety.

Please add the following paragraphs immediately after the paragraph beginning on page 1, line 12:

U.S. Patent Application No. 09/493,942, filed January 28, 2000, claims benefit of U.S. Provisional Application No. 60/117,609, filed January 28, 1999, and claims benefit of U.S. Provisional Application No. 60/136,654, filed May 27, 1999, the disclosures of which are incorporated herein by reference in their entireties.

U.S. Patent Application No. 09/483,551, filed January 14, 2000, claims benefit of U.S. Provisional Application No. 60/116,003, filed January 15, 1999, and claims benefit of U.S. Provisional Application No. 60/117,322, filed January 26, 1999, and claims benefit of U.S. Provisional Application No. 60/122,754, filed February 25, 1999, the disclosures of which are incorporated herein by reference in their entireties.

U.S. Patent Application No. 09/439,101, filed November 12, 1999, claims benefit of U.S. Provisional Application No. 60/108,459, filed November 12, 1998, and claims benefit of U.S. Provisional Application No. 60/108,209, filed November 12, 1998, and claims benefit of U.S. Provisional Application No. 60/108,210, filed November 12, 1998, and claims benefit of U.S. Provisional Application No. 60/117,609, filed January 28, 1999, and claims benefit of U.S. Provisional Application No. 60/136,115, filed May 26, 1999, and claims benefit of U.S. Provisional Application No. 60/136,116, filed May 26, 1999, and claims benefit of U.S. Provisional Application No. 60/136,654, filed May 27, 1999, and claims benefit of U.S. Provisional Application No. 60/159,726, filed October 15, 1999, the disclosures of which are incorporated herein by reference in their entireties.

Please amend the paragraph beginning on page 3, line 17, as follows:

For example, constraint on input levels requires tight automatic gain control ("AGC") of the receiver giving rise to further problems of stability, response time, and maintenance of the required signal level range. Amplifiers with an increased dynamic range are thus desirable in designing receivers to decrease distortion and to relax systems requirements.

Please amend the paragraph beginning on page 3, line 25, as follows:

There is therefore provided in a present embodiment of the invention, a large gain range, high linearity, low noise MOS VGA. An embodiment of the integrated MOS VGA having improved dynamic range comprises a substrate and a first differential pair amplifier disposed upon the substrate. ~~To~~ The first differential pair amplifier is coupled to the VGA output and has a gain that contributes to the VGA gain in direct proportion to the first differential pair amplifier gain.

Please amend the paragraph beginning on page 83, line 5, as follows:

The details of Q enhanced filters are disclosed in more detail in U.S. Patent Application No.[[_____]] 09/573,356 filed [[_____]] May 17, 2000 ~~(B600: 36523)~~ entitled, ~~"CMOS Differential Pair Linearization Technique"~~ "System and Method for Linearizing a CMOS Differential Pair" by Haideh Khorramabadi; based on U.S. Provisional Application No. 60/136,115 filed May 26, 1999 ~~(B600: 34678)~~, the subject matter of which is incorporated in this application in its entirety by reference. Once an improved Q is achieved it is desirable to maintain it over the range of temperatures encountered in circuit operation with temperature compensation circuitry 3206.

Please amend the paragraph beginning on page 108, line 13, as follows:

A more detailed description of the VCO tuning scheme is provided in U.S. Patent Application No.[[_____]] 09/580,014 filed on [[_____]] May 26, 2000 ~~(B600:36226)~~ entitled "System and Method for Narrow Band PLL Tuning" by Ralph Duncan and Tom W. Kwan; based on U.S. Provisional Application No. 60/136,116 filed May 26, 1999 ~~(B600:34677)~~, the subject matter which is incorporated in its entirety by reference. Once the fine, or narrow band PLL has been tuned such that [[is]] it has been locked, its frequency may be used in conjunction with the frequency generated by the coarse PLL to provide channel tuning as previously described for the coarse/fine PLL tuning of FIGS. 21 and 22.

Please amend the paragraph beginning on page 148, line 33, as follows:

VGAs are frequently used to maintain a constant output signal level. VGAs do this by varying the amplifier gain to compensate for varying input levels. In the case of strong or weak signals it is desirable to maintain a linear gain for input ~~verses~~ versus output signals with little noise added. Maintenance of a linear gain reduces distortion for high level input signals. VGAs are often used in IF or RF strips to compensate for prior losses or weak signal reception.

Please amend the paragraph beginning on page 150, line 15, as follows:

The linearization circuit is stimulated by the control signal V_c 7406 ~~is~~ supplied by an external DSP chip. The control signal applied to the linearization circuit 7402 is shaped in a predetermined way. A goal of shaping the control circuit is to produce the second set of control signals 7404 that are applied to the VGA 3403 to produce a desired VGA gain transfer function, measured in decibels, that changes linearly with the applied control signal V_C. In the embodiment shown, V_C is a voltage; however, a control circuit may be equivalently supplied. In an alternate embodiment, the overall transfer function of the VGA is configured to yield a linear function of gain as measured with linear units versus control voltage by appropriately adjusting the linearization circuit through the application of a log to linear conversion current.

Please amend the paragraph beginning on page 152, line 7, as follows:

A V_{ds} control circuit 7504 within the VGA 3403 supplies a V_{ds} control voltage that is applied to nodes 7505 and [[7508]] 7507. The V_{ds} control circuit receives an input VD1 from VD1 control signal generation circuit 7510 that is a part of the linearization circuit 7402. In alternative embodiments, the V_{ds} control circuit is merged into the VD1 control signal generation circuit [[751]] 7510.

Please amend the paragraph beginning on page 152, line 13, as follows:

A current steering circuit 7512 in the gain control circuit 7402 supplies control signals iSig and iAtten. The signal iSig is a control input to the first differential pair amplifier 7500. The signal iAtten is a control input to the second differential pair amplifier [[7500]] 7502.

Please amend the paragraph beginning on page 153, line 21, as follows:

In the first method of V_{ds} control, gain and linearity in the output of the VGA tend to be controlled by adjusting each of four transistors' M4, M10, M13, M14 ~~drain-source~~ drain-to-source voltage ("V_{ds}") of the transistors to control a ~~transductance~~ transconductance ("g_m") associated with each transistor. If a ~~drain-source~~ drain-to-source voltage V_{ds} across a MOSFET device M10, M4, M13, M14 is reduced, a g_m transfer characteristic of that transistor, which is a function of input voltage, becomes flatter. The flatter the g_m transfer function the more linearly the transistor tends to operate[[s]]. The V_{ds} of all four transistors is controlled in order to manipulate an overall g_m characteristic for the VGA.

Please amend the paragraph beginning on page 154, line 26, as follows:

For other size/type transistors this relationship may not hold, but the idea is still applicable. The g_ms of each transistor M10, M4, M13, M14 is controlled to adjust gain. This is accomplished by subtracting[[,]] or adding currents through control lines iSig and iAtten to boost or reduce the VGA g_m, as required. Control signals iSig and iAtten control amplifier gain by adjusting an overall g_m of the amplifier. A fixed available control current is available for controlling VGA gain through the iSig and iAtten control lines. Gain is controlled by selectively steering the available current into the appropriate control line. For large VGA signal inputs, the linearity produced in a VGA from current steering tends to be improved by the addition of the V_{ds} control circuit.

Please amend the paragraph beginning on page 155, line 19, as follows:

VGA operating conditions determine the distribution ~~the~~ of currents iSig and iAtten. When a small signal is applied to the input terminals $+V_{in}$ and $-V_{in}$, it is typically desirable to amplify the signal with a high gain setting. Transistors M10 and M4 are coupled to the differential output so that their g_ms tend to contribute to VGA overall gain. However, transistors M13 and M14 are coupled to the VGA output so that their g_ms tend to decrease VGA gain through a g_m subtraction. Transistors M4 and M10 are controlled by iSig, transistors M13 and M14 are controlled by iAtten.

Please amend the paragraph beginning on page 157, line 7, as follows:

The control voltage V_c 7406 is created by digital circuitry that is responsive to the input level of the amplifier. In the embodiment described, the gain control loop is closed in a digital circuitry domain located off [[of]] chip that produces control signals 7404.

Please amend the paragraph beginning on page 157, line 12, as follows:

The output of the VGA is sampled to determine if sufficient signal strength is available for further signal processing. The sample is processed by an A to D converter into a digital signal, and the control voltage responsive to the level of the VGA output is created. Alternatively, analog methods may be used to sample the output and generate control voltage. In an embodiment, the VGA is utilized as an IF VGA. In alternate embodiments, the VGA is configured for ~~used~~ use at other frequency bands that require an adjustment in gain.

Please amend the paragraph beginning on page 158, line 16, as follows:

A transistor M1 has its source coupled to node 7505, its drain comprises the $+I_{out}$ terminal of the VGA. The gate of transistor M1 is coupled to the positive output of U1. A transistor M2 has its source coupled to 7507, its drain comprises the $-I_{out}$ terminal of the VGA. The gate of transistor M2 is coupled to the negative output of [[A1]] U1.

Please amend the paragraph beginning on page 159, line 3, as follows:

The source of M13 and M14 are coupled in common to node 7503 and to the control signal iAtten. Control signal iAtten tends to cause a decrease in amplifier gain, while control signal iSig tends to increase amplifier gain. The sources of M10 and M4 are coupled in common to iSig at node [[7510]] 7501. The drains of M10 and M13 are coupled in common to provide an output signal $+I_{out}$. The drains of M4 and M14 are coupled in common to provide an output signal $-I_{out}$. In the exemplary embodiment, input $-V_{in}$ is coupled to the gates of M10 and M14. Input $+V_{in}$ is coupled to the gates of M4 and M13. In the exemplary embodiment, differential inputs and outputs are shown in the amplifier. However, it is understood by those skilled in the art that a single ended configuration is equivalently produced by the use of a device such as a balun.

Please amend the paragraph beginning on page 159, line 26, as follows:

FIG. 78b is a graph of g_m ~~verses~~ versus V_{gs} as V_{ds} is varied from 50 mV to 1 V. To provide improved output linearity performance, it is desirable to operate a transistor on a curve of g_m that has a constant value and zero slope. As seen in the graph for a V_{ds} of approximately 50 mV, the curves of g_m ~~verses~~ versus V_{gs} tend to be flat. As V_{ds} is increased, the curve begins to slope, indicating the presence of non-linearity in the output signal. As V_{ds} increases, the curve not only begins to slope, but it develops a bow, further complicating the compensation for the non-linearities at the higher level of V_{ds}. These irregularities in g_m tend to be the sources of non-linearities in the output of the amplifier. Thus, it is desired to provide a flat g_m response to produce a more linear transfer function for the VGA by controlling V_{ds}.

Please amend the paragraph beginning on page 160, line 7, as follows:

FIG. 78c is a graph of the cross-section of FIG. 78b plotting g_m ~~verses~~ versus V_{ds} for various values of V_{gs}. As V_{ds} changes from approximately 200 mV to 500 mV, g_m changes from approximately 5 mS to 13 mS. The change in g_m from 5 mS to 13 mS by changing V_{ds} may be used to control gain. Thus, as V_{ds} is decreased, the gain is decreased. Control of V_{ds} provides approximately 9 dB of gain control range.

Please amend the paragraph beginning on page 162, line 20, as follows:

FIG. 80 is a schematic of a VD1 control signal generation circuit. Control signal V_c is fed to the positive input of a differential amplifier U2. ~~Signal~~ Single ended output of amplifier U2 is fed into the gate of transistor MC9. The source of MC9 is connected to the negative input of U2. The source of MC9 is also coupled to a first terminal of a resistor R1. A second terminal of R1 is coupled to ground. The drain of MC9 receives a current i_{c1} that is supplied by a drain of transistor MC7. The source of MC7 is coupled to a supply voltage V_{cc}. The gate of MC7 is coupled to the gate of [[MC6]] MC8. The source of [[MC6]] MC8 is coupled to a supply voltage V_{cc}. The drain of [[MC6]] MC8 is coupled to a first terminal of a resistor R2. The second terminal of resistor R2 is coupled to node [[1001]] 7501. The node formed by coupling [[MC6]] MC8 to R2 supplies control signal VD1. Together transistors MC7 and [[MC6]] MC8 form a current mirror 8001.

Please amend the paragraph beginning on page 163, line 3, as follows:

Control current V_c sets up the control current i_{c1} through amplifier U2, resistor R1 and transistor MC9. Current i_{c1} is mirrored through transistor MC7 and MC8 of the current mirror 8001. The current generated in the drain lead of [[MC6]] MC8 creates a voltage across resistor R2 as reference to the voltage present in node 7501. Thus, R1 and R2 are sized properly to control V_{ds} across M10, M4, M13 and M14. For example, VD1 can range from 100mV to 600mV. This condition corresponds to a V_c = [[05V]] 0.5V at a minimum gain, maximum input condition and a V_c = 2.5V at a maximum gain, minimum input signal condition.

Amendments to the Figures

Please substitute the attached replacement of Figure 78c for pending Figure 78c. An annotated copy is also included to show the change made. Specifically, element reference number "401" is corrected to read "7801" to be in conformity with the specification as originally filed, as shown in the attached annotated drawing sheet.

Please substitute the attached replacement of Figure 79 for pending Figure 79. An annotated copy is also included to show the change made. Specifically, element reference number "8010" is corrected to read "7510" to be in conformity with the specification as originally filed, as shown in the attached annotated drawing sheet.

Please substitute the attached replacement of Figure 80 for pending Figure 80. An annotated copy is also included to show the change made. Specifically, element reference number "MC6" is corrected to read "MC8" in order to avoid duplicate figure element reference numbers in Figures 79 and 80, as shown in the attached annotated drawing sheet.